

# READEX

Runtime Exploitation of Application Dynamism for Energy-efficient eXascale Computing

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TU Dresden, Center for Information Services and High Performance Computing

- FET-HPC project, launched 09/2015
- [www.readex.eu](http://www.readex.eu)
- Technische Universität Dresden/ZIH (Coordinator)
- Norges Teknisk-Naturvitenskapelige Universitet
- Technische Universität München
- IT4Innovations, VSB-Technical University of Ostrava
- Irish Centre for High-End Computing
- Intel Corporation SAS
- Gesellschaft für numerische Simulation mbH



IT4Innovations  
national  
supercomputing  
center

# Motivation

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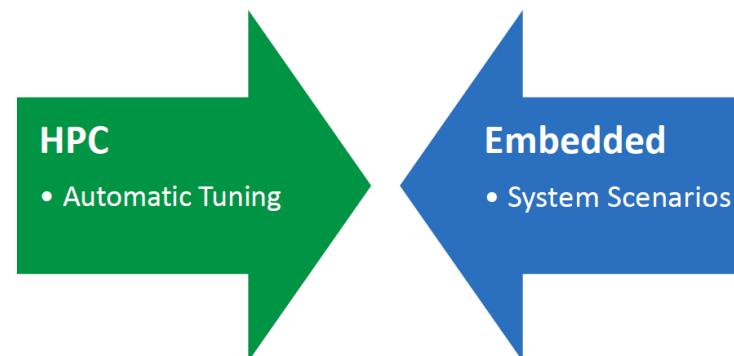
- Energy is critical to current and future systems
- Applications exhibit dynamic behaviour
  - Changing resource requirements
  - Changing load on processors over time

Create a tools-aided methodology for automatic tuning for energy efficiency in HPC

- Dynamically adjust system parameters to actual resource requirements

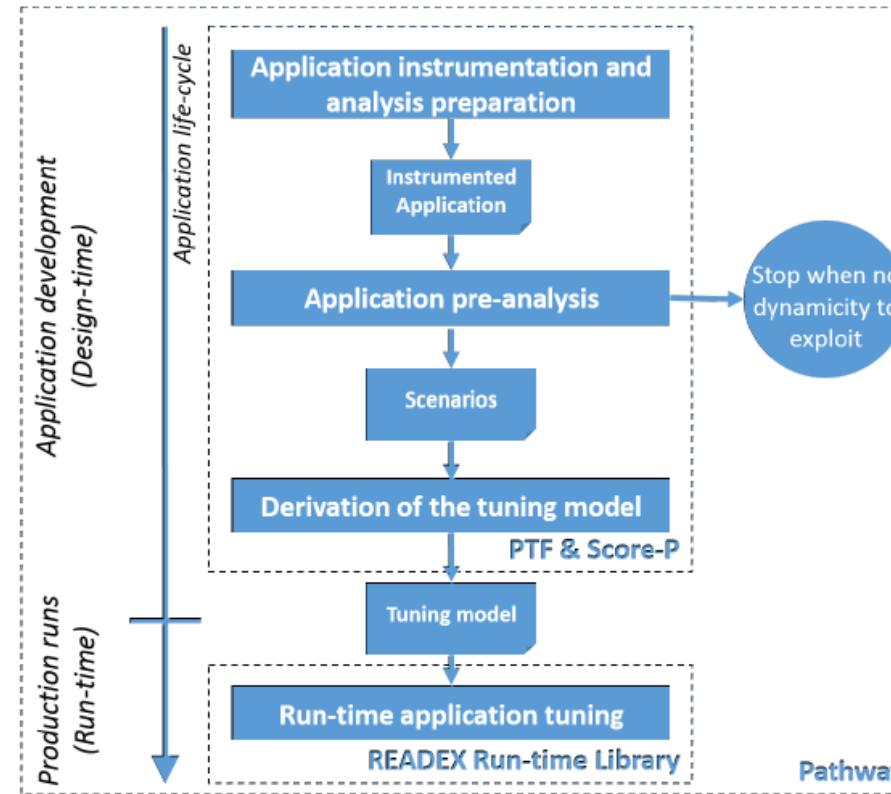
Join technologies from embedded systems and HPC

- HPC: PTF, Score-P, and HDEEM
- ES: System scenario methodology



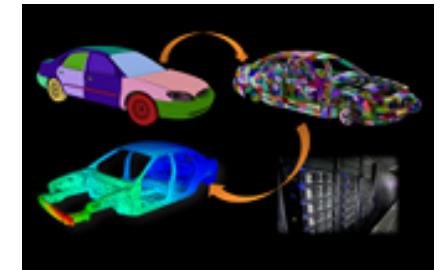
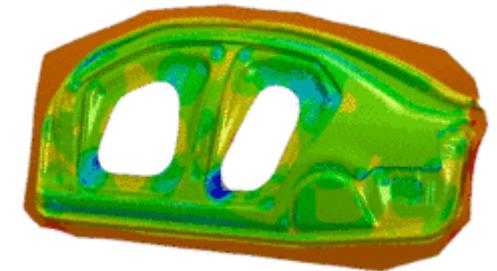
# READEX: Overview

High-level view of READEX tools-aided methodology



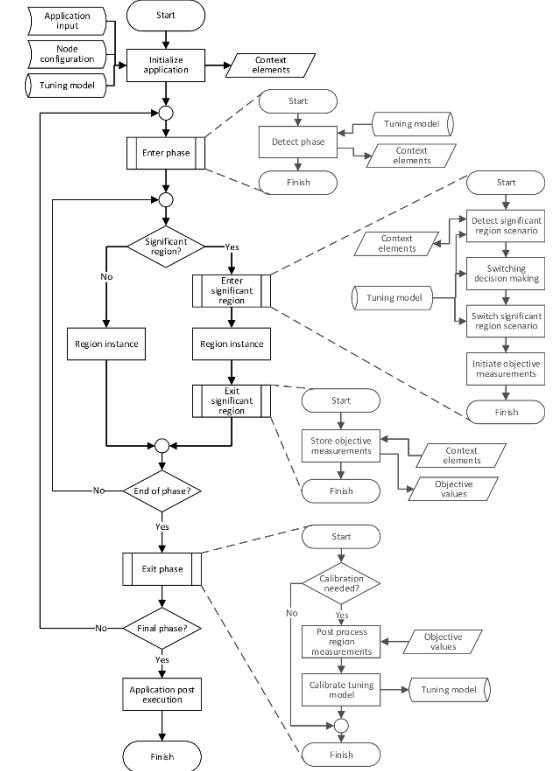
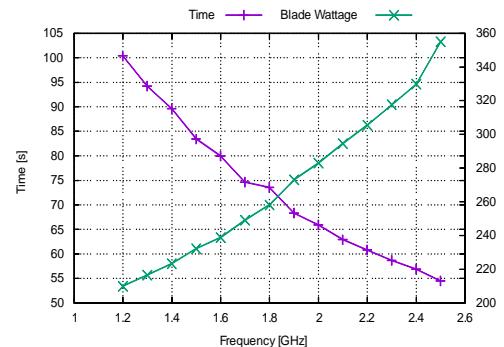
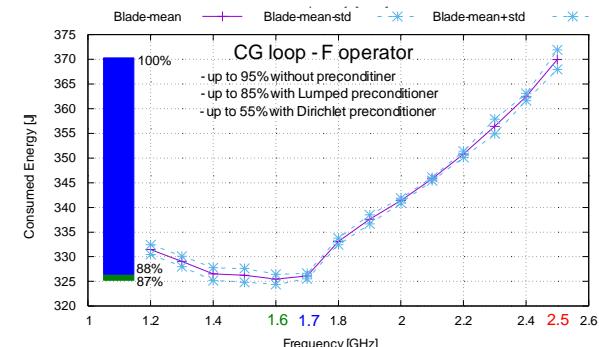
## Co-design approach

- Manual tuning for energy-efficiency as a baseline
- Automatic tuning for comparison
- Applications
  - PERMON and ESPRESO (FETI tools from IT4Innovations)
  - Indeed (GNS)
  - CORAL benchmark suite



# Current Status

- First Milestones achieved
  - Dissemination Strategy
  - System Parameters
- Formalised methodology
- READEX tool-suite design and implementation
- Manual tuning efforts



# Dissemination

- International Workshop on Code Auto-Tuning (DCAT) workshop @ CGO'16
    - Invited speakers, ~20 participants
  - Dissemination material (SC'15)
  - Presentations
    - Keynote on READEX at ICGHPC 2016
    - GAMM DMV yearly meeting
  - Posters
    - CSE 2015, Porto
    - HiPEAC conference 2016, Prague
  - Publications
  - Outreach into HiPEAC, PRACE, EE-HPC-WG, System Scenario SIG

**Partners**

**Funding and Contact**

**READEX**  
Runtime Exploitation of Application Dynamism  
From Software to Hardware via KAscale Computing  
[www.readex.eu](http://www.readex.eu)

• Technische Universität Dresden  
• Technische Universität Ilmenau  
• University of Applied Sciences Brandenburg  
• Institute of Technology and Business University of Osnabrück  
• Chair for Microprocessor Design  
• Chair for Logic Design  
• Institute for Future Computing Architectures

• Institut für Mikroelektronik und Mikrosysteme (IMM) der Universität Regensburg  
• Institute for Microelectronics and Microsystems (IMM) of the University of Regensburg  
• Institute for Microelectronics and Microsystems (IMM) of the University of Regensburg

Project Name:  
2010-09-22 16:16

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**Runtime Exploitation of Application Dynamism for Energy-efficient KAscale computing**

**TECHNISCHE UNIVERSITÄT DRESDEN**

**TUM**

**JKU**  
JKU Linz  
NUCLEUS

**NTNU**  
gns

**intel**

**READEX**  
Runtime application  
exploitation  
for  
Energy Efficient  
KAscale computing

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for Energy-Efficient Exascale Computing

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## RUNTIME EXPLOITATION OF APPLICATION DYNAMISM FOR ENERGY-EFFICIENT EXASCALE COMPUTING

### OVERVIEW

- Future exascale systems of HPC applications to achieve improved performance and efficiency
- Dynamic application behaviour is a key feature of future systems
- Bring together application experts, system experts and domain experts
- Bring together application experts, system experts and domain experts

### SYSTEM SCENARIO METHODOLOGY

- Start design phase by forming dynamic application design approach
- Identify system requirements and system architecture
- Design the system architecture employing model creation
- Design the system architecture employing model creation e.g., system simulation
- Create system architecture employing model creation
- Create system architecture employing model creation
- Create system architecture employing model creation
- Run system architecture prediction using identifier learned by system architecture prediction
- Run system architecture prediction using identifier learned by system architecture prediction
- Identify system requirements and system architecture
- Identify system requirements and system architecture
- Run system architecture prediction using identifier learned by system architecture prediction
- Run system architecture prediction using identifier learned by system architecture prediction
- Run system architecture prediction using identifier learned by system architecture prediction
- Run system architecture prediction using identifier learned by system architecture prediction

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graph TD
    A[Start design phase by forming dynamic application design approach] --> B[Identify system requirements and system architecture]
    B --> C[Design the system architecture employing model creation]
    C --> D[Create system architecture employing model creation]
    D --> E[Run system architecture prediction using identifier learned by system architecture prediction]
    E --> F[Identify system requirements and system architecture]
    F --> G[Run system architecture prediction using identifier learned by system architecture prediction]
    G --> H[Create system architecture employing model creation]
    H --> I[Run system architecture prediction using identifier learned by system architecture prediction]
    I --> J[Identify system requirements and system architecture]
    J --> K[Run system architecture prediction using identifier learned by system architecture prediction]
    K --> L[Create system architecture employing model creation]
    L --> M[Run system architecture prediction using identifier learned by system architecture prediction]
    M --> N[Identify system requirements and system architecture]
    N --> O[Run system architecture prediction using identifier learned by system architecture prediction]
    O --> P[Create system architecture employing model creation]
    P --> Q[Run system architecture prediction using identifier learned by system architecture prediction]
    Q --> R[Identify system requirements and system architecture]
    R --> S[Run system architecture prediction using identifier learned by system architecture prediction]
    S --> T[Create system architecture employing model creation]
    T --> U[Run system architecture prediction using identifier learned by system architecture prediction]
    U --> V[Identify system requirements and system architecture]
    V --> W[Run system architecture prediction using identifier learned by system architecture prediction]
    W --> X[Create system architecture employing model creation]
    X --> Y[Run system architecture prediction using identifier learned by system architecture prediction]
    Y --> Z[Identify system requirements and system architecture]
    Z --> AA[Run system architecture prediction using identifier learned by system architecture prediction]
    AA --> BB[Create system architecture employing model creation]
    BB --> CC[Run system architecture prediction using identifier learned by system architecture prediction]
    CC --> DD[Identify system requirements and system architecture]
    DD --> EE[Run system architecture prediction using identifier learned by system architecture prediction]
    EE --> FF[Create system architecture employing model creation]
    FF --> GG[Run system architecture prediction using identifier learned by system architecture prediction]
    GG --> HH[Identify system requirements and system architecture]
    HH --> II[Run system architecture prediction using identifier learned by system architecture prediction]
    II --> JJ[Create system architecture employing model creation]
    JJ --> KK[Run system architecture prediction using identifier learned by system architecture prediction]
    KK --> LL[Identify system requirements and system architecture]
    LL --> MM[Run system architecture prediction using identifier learned by system architecture prediction]
    MM --> NN[Create system architecture employing model creation]
    NN --> OO[Run system architecture prediction using identifier learned by system architecture prediction]
    OO --> PP[Identify system requirements and system architecture]
    PP --> QQ[Run system architecture prediction using identifier learned by system architecture prediction]
    QQ --> RR[Create system architecture employing model creation]
    RR --> SS[Run system architecture prediction using identifier learned by system architecture prediction]
    SS --> TT[Identify system requirements and system architecture]
    TT --> UU[Run system architecture prediction using identifier learned by system architecture prediction]
    UU --> VV[Create system architecture employing model creation]
    VV --> WW[Run system architecture prediction using identifier learned by system architecture prediction]
    WW --> XX[Identify system requirements and system architecture]
    XX --> YY[Run system architecture prediction using identifier learned by system architecture prediction]
    YY --> ZZ[Create system architecture employing model creation]
    ZZ --> AA
  
```

### READEX DESIGN AND METHODOLOGY

- Activities: design, run, predict and validate at runtime
- Design: run an analysis based on known, user-defined system requirements and system architecture
- Run: validate the system architecture
- Predict: identify system requirements and system architecture
- Validate: validate system requirements and system architecture

```

graph TD
    A[Activities: design, run, predict and validate at runtime] --> B[Design: run an analysis based on known, user-defined system requirements and system architecture]
    B --> C[Run: validate the system architecture]
    C --> D[Predict: identify system requirements and system architecture]
    D --> E[Validate: validate system requirements and system architecture]
    E --> F[Activities: design, run, predict and validate at runtime]
  
```

### PERSPECTIVE TUNING FRAMEWORK

- Integrating multiple tuning approaches
- Different approaches for different tuning goals
- Different approaches for pre/post training
- Different approaches for different system requirements
- Differentiated in the READEX project
- Tuning for performance, energy efficiency, reliability, and system健壮性

Diagram showing a central tuning interface connected to various tuning modules: Performance Tuning, Energy Efficiency Tuning, Reliability Tuning, and System健壮性 Tuning.

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Horizon 2020 European Union Funding for Research & Innovation

**TECHNISCHE UNIVERSITÄT DRESDEN** **IEE** **TUM** **VIENNA GRIDLAB** **GEODANICA AIR SYSTEMS GMBH** **HTWK** **NTNU**



# Integration with the Ecosystem

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- International Workshop on Code Auto-Tuning (DCAT)
  - Extensions to Score-P
  - ESPRESO/PERMON tuning efforts
  - Automatic energy-efficiency tuning
- 
- HDEEM system Taurus open to all interested projects
    - High definition energy-measurement system (1000 Sa/s, accuracy validated)

## Activities:

- External Advisory Board
  - UTK, VA Tech, LLNL, Skoda, imec, JSC
- International Workshop on Code Auto-Tuning (DCAT) @ CGO'16
- Visiting researcher from St Xaviers Catholic College in India at TUM

## Support by EXDCI?

- Cross-border call for proposals
- Organization of workshops
- Funding for visiting researchers

# Role in Extreme Scale Demonstrator

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- Willing to provide input to ESD proposal
- Provide product quality performance and energy-efficiency tools
- Energy-efficiency crucial for ESD
  - READEX will contribute to energy-efficiency tuning
- What will the role of software be in the ESD?

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## Questions?

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